

WHAT IS CLAIMED IS:

1. A method for controlling a phase locked loop in a computer system clock
2 generator comprising the steps of:

3 generating a lead error signal when a first signal leads a second signal and a lag
4 error signal when said first signal lags said second signal;

5 generating a phase error signal in response to said lead error signal and said lag
6 error signal;

7 generating a variable first gain signal in response to said phase error signal and
8 said first signal;

9 generating a variable second gain signal in response to said lead error signal and
10 said lag error signal;

11 generating a control signal in response to a first reference signal, a second
12 reference signal, said first gain signal and said second gain signal; and

13 applying said control signal to a voltage controlled oscillator as a frequency
14 control signal of an output of a voltage controlled oscillator generating said second
15 signal.

1. The method of claim 1, wherein said lead error signal is a logic one pulse if said
2 first signal leads said second signal during a cycle of said second signal and said lag error
3 signal is a logic one pulse if said first signal lags said second signal during said cycle of
4 said second signal.

1. The method of claim 1, wherein said phase error signal is increased on a
2 transition of said lead error signal and decreased on a transition of said lag error signal.

1 4. The method of claim 1, wherein said first gain signal is increased if an absolute
2 value of said phase error signal reaches a first threshold value within a time window and
3 decreased if said absolute value of said phase error signal does not reach said first
4 threshold value in said time window.

1 5. The method of claim 1, wherein said second gain signal is a value $+K$ if said lead
2 error signal is a logic one pulse and a value $-K$ if said lag error signal is a logic one pulse,
3 wherein K is a numerical value including the value one.

1 6. The method of claim 1, wherein said first gain signal is limited to a magnitude
2 between a predetermined maximum level and a predetermined minimum level.

1 7. The method of claim 6, wherein a third signal is generated by adding said first
2 reference signal to said second reference signal multiplied by said first gain signal.

1 8. The method of claim 7, wherein said control voltage is generated in response to
2 said third signal, an integral of said third signal, and said second gain signal.

1 9. The method of claim 8, wherein said third signal is multiplied by said second gain
2 signal generating a modified third signal.

1 10. The method of claim 9, wherein said control voltage is generated by adding said
2 modified third signal multiplied by a first constant to an integral of said modified third
3 signal multiplied by a second constant.

1 11. The method of claim 1, wherein said first threshold value and said time window
2 are dynamically variable.

PRINTED IN U.S.A. 03/20/2024

1 12. A phase locked loop (PLL) comprising:

2 a phase comparator receiving a first signal and a second signal and generating a
3 lead error signal when said first signal leads said second signal and a lag error signal
4 when said first signal lags said second signal;

5 a phase error generator for generating a phase error signal in response to said lead
6 error signal and said lag error signal;

7 a circuit for generating a variable first gain signal in response to said phase error
8 signal and said first signal;

9 a circuit for generating a variable second gain signal in response to said lead error
10 signal and lag error signal;

11 a circuit for generating a control signal in response to a first reference signal, a
12 second reference signal, said first gain signal and said second gain signal; and

13 a voltage controlled oscillator receiving said control signal as a frequency control
14 signal of an output of said voltage controlled oscillator generating said second signal.

1 13. The PLL of claim 12, wherein said lead error signal is a logic one pulse if said
2 first signal leads said second signal during a cycle of said second signal and said lag error
3 signal is a logic one pulse if said first signal lags said second signal during said cycle of
4 said second signal.

1 14. The PLL of claim 12, wherein said phase error signal is increased on a transition
2 of said lead error signal and decreased on a transition of said lag error signal.

1 15. The PLL of claim 12, wherein said first gain signal is increased if an absolute
2 value of said phase error signal reaches a first threshold value within a time window and

3 decreased if said absolute value of said phase error signal does not reach said first
4 threshold value in said time window.

1 16. The PLL of claim 12, wherein said second gain signal is a value $+K$ if said lead
2 error signal is a logic one pulse and a value $-K$ if said lag error signal is a logic one pulse,
3 wherein K is a numerical value including the value one.

1 17. The PLL of claim 12, wherein said first gain signal is limited to a magnitude
2 between a predetermined maximum level and a predetermined minimum level.

1 18. The PLL of claim 17, wherein a third signal is generated by adding said first
2 reference signal to said second reference signal multiplied by said first gain signal.

1 19. The PLL of claim 18, wherein said control voltage is generated in response to
2 said third signal, an integral of said third signal, and said second gain signal.

1 20. The PLL of claim 19, wherein said third signal is multiplied by said second gain
2 signal generating a modified third signal.

1 21. The PLL of claim 20, wherein said control voltage is generated by adding said
2 modified third signal multiplied by a first constant to an integral of said modified third
3 signal multiplied by a second constant.

1 22. The PLL of claim 12, wherein said first threshold value and said time window are
2 dynamically variable.

1 23. A data processing system comprising:
2 a processor central processing unit (CPU);
3 a random access memory (RAM);
4 a read only memory (ROM); and
5 a bus system coupling said CPU to said ROM and said RAM, said CPU further
6 comprising a phase locked loop (PLL) in clock generator, said PLL comprising:
7 circuitry for receiving a first signal and a second signal and generating a lead error
8 signal when said first signal leads said second signal and a lag signal when said first
9 signal lags said second signal;
10 circuitry for generating a phase error signal in response to said lead error signal
11 and said lag error signal;
12 circuitry for generating a variable first gain signal in response to said phase error
13 signal;
14 circuitry for generating a variable second gain signal in response to said lead error
15 signal and lag error signal;
16 circuitry for generating a control signal in response to a first reference signal, a
17 second reference signal, said first gain signal and said second gain signal; and
18 a voltage controlled oscillator receiving said control signal as a frequency control
19 signal for an output of said voltage controlled oscillator generating said second signal.

1 24. The data processing system of claim 23, wherein said lead error signal is a logic
2 one pulse if said first signal leads said second signal during a cycle of said second signal
3 and said lag error signal is a logic one pulse if said first signal lags said second signal
4 during said cycle of said second signal.

1 25. The data processing system of claim 23, wherein said phase error signal is
2 increased on a transition of said lead error signal and decreased on a transition of said lag
3 error signal.

1 26. The data processing system of claim 23, wherein said first gain signal is increased
2 if an absolute value of said phase error signal reaches a first threshold value within a time
3 window and decreased if said absolute value of said phase error signal does not reach
4 said first threshold value in said time window.

1 27. The data processing system of claim 23, wherein said second gain signal is a
2 value $+K$ if said lead error signal is a logic one pulse and a value $-K$ if said lag error
3 signal is a logic one pulse, wherein K is a numerical value including the value one.

1 28. The data processing system of claim 23, wherein said first gain signal is limited
2 to a magnitude between a predetermined maximum level and a predetermined minimum
3 level.

1 29. The data processing system of claim 28, wherein a third signal is generated by
2 adding said first reference signal to said second reference signal multiplied by said first
3 gain signal.

1 30. The data processing system of claim 29, wherein said control voltage is generated
2 in response to said third signal, an integral of said third signal, and said second gain
3 signal.

1 31. The data processing system of claim 30, wherein said third signal is multiplied
2 by said second gain signal generating a modified third signal.

1 32. The data processing system of claim 31, wherein said control voltage is generated
2 by adding said modified third signal multiplied by a first constant to an integral of said
3 modified third signal multiplied by a second constant.

PRINTED IN U.S.A. 100-1000